NEURON® 3150™ CHIP External Memory Interface

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Introduction

The NEURON 3150 CHIP provides an external memory bus to permit expansion of memory up to 58K bytes beyond the 512 bytes of EEPROM and 2K bytes of RAM resident on the chip. The NEURON 3150 CHIP requires 16K bytes of external non-volatile memory to store its firmware. The remaining 42K bytes of external memory are available for user application program and data. The external memory may be implemented using various combinations of ROM, EPROM, NVRAM, and static RAM devices.

The NEURON 3120™ CHIP, which has a masked ROM firmware image and no external memory bus, may provide enough on-chip memory resources (512 bytes of EEPROM and 1K byte of RAM) for simpler applications. The NEURON 3120 CHIP targets applications requiring minimum node cost.

The focus of this engineering bulletin is the NEURON 3150 CHIP memory expansion bus. It describes (i) a strategy to assess memory requirements for a given application, (ii) logical function of the memory interface pins, (iii) timing requirements, and (iv) three memory design examples.

Assessing Memory Requirements

LONWORKS nodes based on the NEURON 3150 CHIP use a combination of three different types of memory:

Non-Volatile Memory for NEURON CHIP Firmware: 16K bytes of external non-volatile memory, beginning at address 0, is needed to maintain a permanent copy of the NEURON CHIP firmware. This memory should be mapped to 0000-3FFFH, and should be decoded for read operations only. Additional non-volatile memory may contain application code and constants. This memory may use ROM, EPROM, EEPROM, or NVRAM technology.

Electrically Rewriteable Non-Volatile Memory for Network and Application Information: The NEURON 3150 CHIP provides 512 bytes of on-chip EEPROM to store network and system configuration and user applications. EEPROM technology is used for this memory space since the configuration data and applications programs and constants can be configured and modified in-system. External EEPROM or non-volatile RAM may be added on the 3150 chip memory bus if more space is needed for the applications programs and constants.

Read/Write Memory for Packet Buffering: The NEURON 3150 CHIP contains 2K bytes of on-chip RAM. This internal RAM is used for network packet buffering and for application data space. External static RAM (SRAM) may be added to a NEURON 3150 CHIP memory bus if more packet buffering or application data space is required.

A LONWORKS application node may include the external memory types described above by partitioning the available 58K byte memory space into three distinct regions aligned on 256-byte page boundaries. The different memory types do not need to map to contiguous address space. However, the LONBUILDER™ NEURON C compiler enforces the ordering of the types of memory to be ROM/EPROM first, EEPROM second, and finally RAM. The NEURON C compiler and LONBUILDER linker locate parts of an application in appropriate memory regions (see Chapter 6 of the *NEURON C Programmer's Guide).*

The LONBUILDER system generates a detailed report of the memory usage in the BUILD.LOG file when the `Output Link Summary` project option is enabled (see Chapter 4 of the *LONBUILDER User's Guide).*

There are many elements of a LONWORKS application which affect the amount of each type of memory required. Network configuration, the number of network variables, communication buffer parameters, and application code go into the calculation. For any given application, the executable code for the NEURON CHIP's stack-based architecture is typically smaller than executable code for register-based microcontroller architectures. As a rule-of-thumb, one can expect roughly six or seven bytes of executable code per line of NEURON C code. It is always best to create test applications using the LONBUILDER Workbench to determine exact requirements.

The LONBUILDER system can logically emulate an intended memory configuration to permit evaluation of an application's memory requirements before committing to custom hardware. Chapter 6 of the *LONBUILDER User's Guide* explains how to define the memory layout of the target node.

The LONBUILDER system linker determines the appropriate locations for system code, application code, constants, and data, based on the hardware properties assigned by the system designer to the emulator as well as explicit segment definition keywords included in the application code. It is not necessary to create detailed linker command files to map application elements to various memory regions. The LONBUILDER system keeps track of the necessary details to make correct decisions about memory allocation.

It is important to note that write cycles to EEPROM memory take up to 20 ms, during which time subsequent read or write cycles accessing address space mapped into the same EEPROM device cannot occur. If the NEURON 3150 CHIP firmware is loaded into the same EEPROM device as application code, this will cause a lockout and lead to unpredictable results when the network and media access control processors of the NEURON 3150 CHIP try to fetch instructions during these 20 ms periods. Therefore, when using EEPROM for system firmware and applications code, separate devices should be used for the two types of code.

External Memory Design Considerations

The following sections address the logical interfacing as well as the AC timing considerations for external memory design.

Memory Interface Logical Description

Figure 1 shows the memory map of the NEURON 3150 CHIP. Memory locations from 0 to E7FFH are external to the NEURON 3150 CHIP. Access to this memory is through an external memory bus consisting of eight bi-directional three-state data lines, 16 unidirectional address lines driven by the NEURON 3150 CHIP, and three control lines. Figure 2 shows the pinout of the NEURON 3150 CHIP.

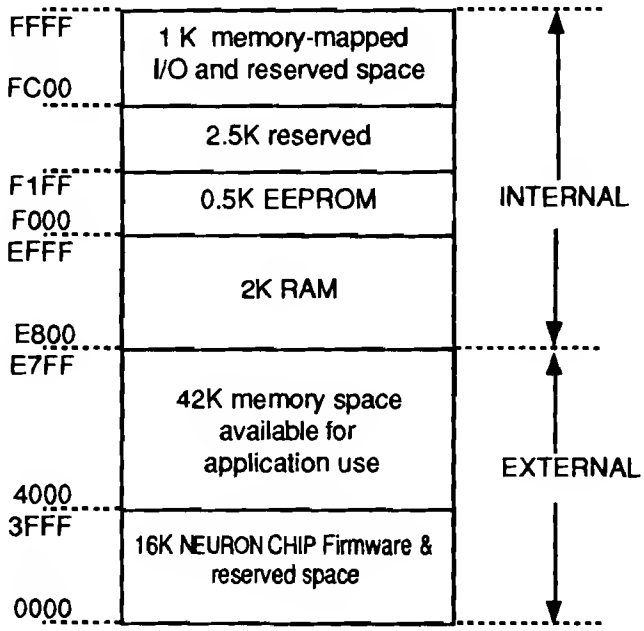

Figure 1. The NEURON 3150 CHIP memory map.

Two of the three control lines are used for the external memory interface.

~E Enable Clock - This output is a strobe driven by the NEURON 3150 CHIP to synchronize the external bus. Its frequency is one-half that of the input clock or crystal. ~E is low during the second half of the memory cycle, which indicates that the NEURON 3150 CHIP is actively reading or writing data. During write cycles, the NEURON 3150 CHIP drives the new data onto the data bus during the time ~E is low. During read cycles, the NEURON 3150 CHIP clocks the external data in on the low-to-high transition of ~E.

R/~W Read/Write - This output indicates the direction of the data bus. It is set by the NEURON 3150 CHIP to high during a Read cycle, and low on a Write cycle. R/~W changes state during the time ~E is high, and is stable during the time ~E is low.

The third control pin on the NEURON 3150 CHIP is reserved. It must be treated as follows:

~XD This input must be tied high.

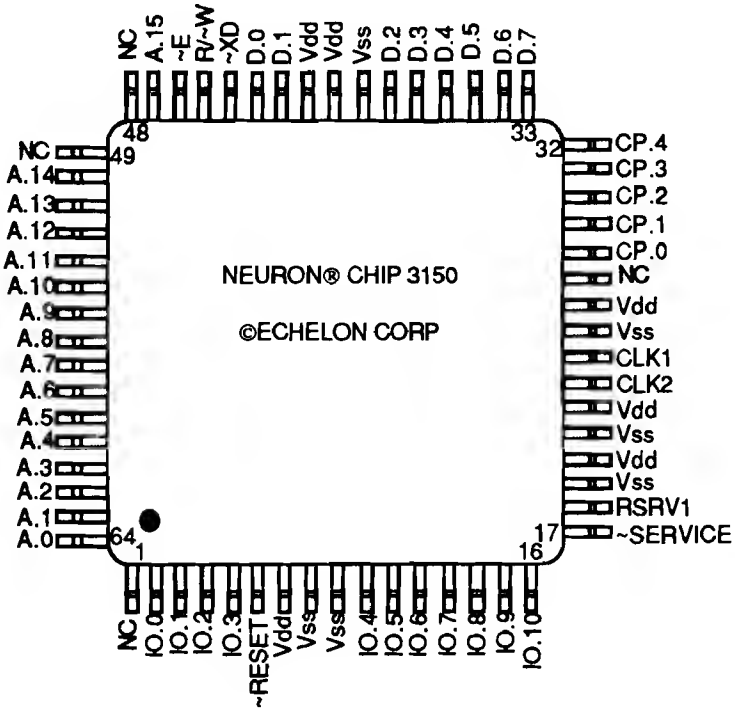

Figure 2. NEURON 3150 CHIP pinout.

Timing Requirements

The NEURON CHIP includes three independent processors sharing a common memory bus. The three processors execute in a rigid pipelined sequence. As a result, the NEURON CHIP can initiate a memory operation on every processor cycle. A processor cycle is defined as two input clock periods. Memory wait states are not supported. Therefore, memory or memory-mapped I/O devices must respond within the access time dictated by the NEURON 3150 CHIP processor cycle time.

Figures 3 and 4 show guaranteed timing for read and write access to external memory under worst-case conditions. Tables 1 and 2 show the effect that restricting the tolerance of the power supply voltage to ±5% has on the timing parameters.

Memory timing requirements for read operations are driven by two fixed timing parameters, the address valid delay (t_{AD} in figure 3) measured from the start of the memory cycle and read data setup time (t_{DSR} in figure 3) measured back from the end of the memory cycle.

The memory access time (t_{ACC}) requirement is derived using the following equation:

$$t_{ACC} = t_{CYC} - t_{AD} - t_{DSR}$$

The NEURON CHIP supports a maximum input clock frequency of 10 MHz. This translates to a processor cycle time of 200 ns. To specify a read-only memory device, the previous formula is used to derive a memory access time requirement of 79 ns for 10 MHz NEURON 3150 CHIP operation. The nearest industry-standard access speed for EPROM devices meeting this requirement is 70 ns. If the same calculation is done for a design using a ±5% power supply, the access speed of the memory is relaxed to 90 ns (see table 1).

Many applications do not require the NEURON 3150 CHIP to run at 10 MHz. Reducing the input clock to 5 MHz relaxes the access time constraints significantly. The 126 ns address valid plus read data set up time delay remains the same, but now the total cycle time is 400 ns instead of 200 ns. The external memory's address access speed requirement is now 400 - 38 - 83 = 274 ns. The corresponding industry-standard speed is 250 ns.

A memory design including external RAM requires careful examination of figure 3, and tables 1 and 2. RAM devices latch data on the rising edge of the write enable signal. Static RAM and non-volatile RAM devices demand an address hold time (T_{AD}) of 0-20 ns beyond the rising edge of the write enable. The second design example describes a solution to achieve the address hold time required by static RAM devices.

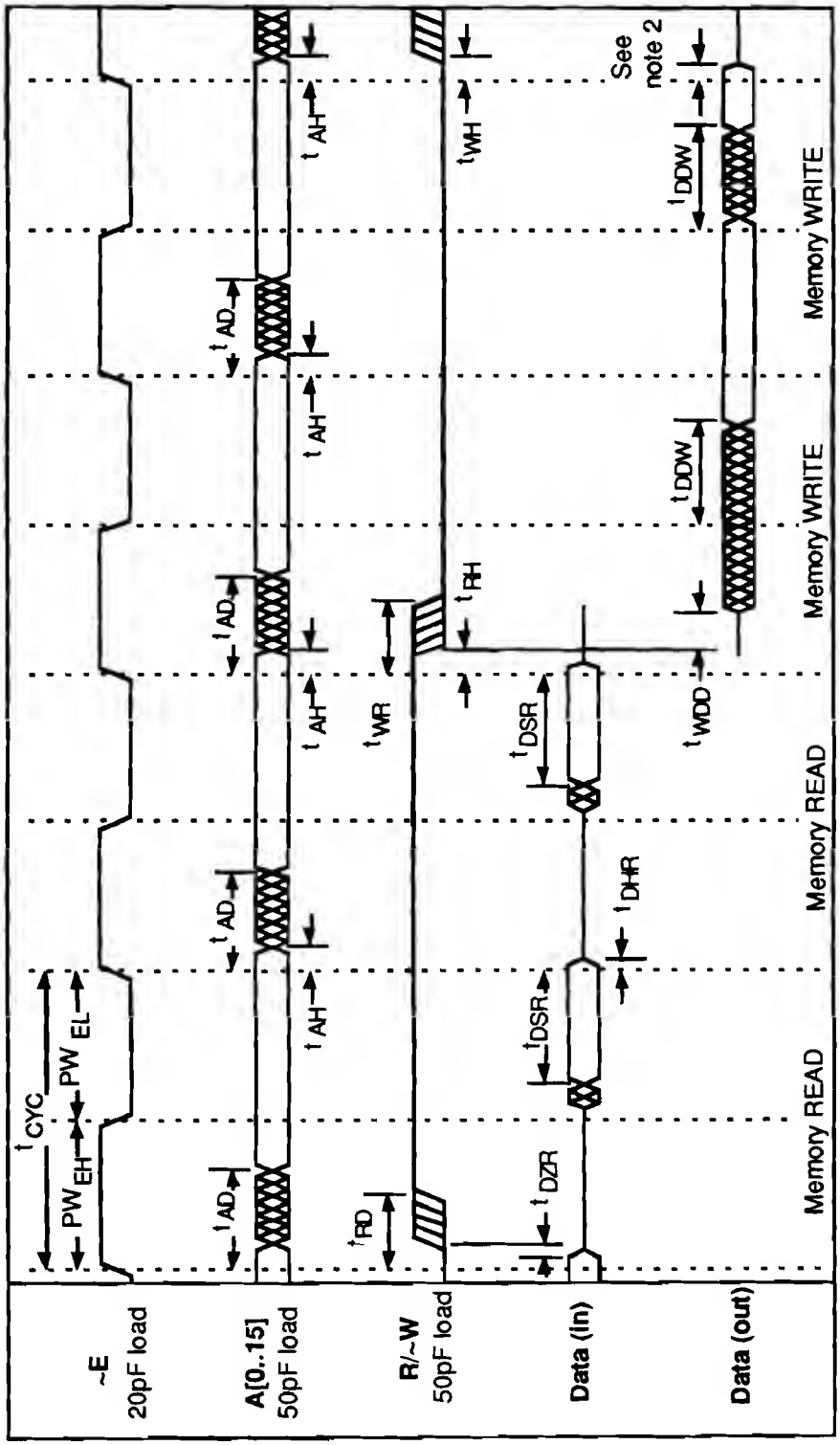

Figure 3. NEURON 3150 CHIP memory interface timing diagram.Table 1.

NEURON 3150 CHIP memory timings (worst-case @ 4.5V, 70°C).

Symbol	Parameter	Min	Max	Unit
t_{CYC}	Memory cycle time[1]	200	3200	ns
PW_{EH}	Pulse width ~E High	$t_{CYC/2} - 5$	$t_{CYC/2} + 5$	ns
PW_{EL}	Pulse width ~E low	$t_{CYC/2} - 5$	$t_{CYC/2} + 5$	ns
t_{AD}	Delay, ~E High to address valid	-	38	ns
t_{AH}	Address hold time	5	-	ns
t_{RD}	Delay, ~E high to R/~W valid (read cycle)	-	25	ns
t_{RH}	R/~W hold time (read cycle)	5	-	ns
t_{DSR}	Read data setup time	83	-	ns
t_{DZR}	Delay data bus high-Z to R/~W high	5	-	ns
t_{DHR}	Data hold time (read cycle)	0	-	ns
t_{WR}	Delay, ~E high to R/~W valid (write cycle)	-	25	ns
t_{WDD}	Delay, R/~W low to NEURON CHIP data drivers ON	10	-	ns
t_{DDW}	Delay, ~E Low to data valid	-	67	ns
t_{WH}	R/-W hold time (write cycle)[2]	5	-	ns

Notes:

1. $t_{cyc} = 2 \times 1/f$, where 'f' is the input clock frequency at CLK1. Valid values of 'f' are 10, 5, 2.5, 1.25, and .625 MHz.
2. If a write cycle is followed by a read cycle, the data bus goes to the high-impedance state at the beginning of the read cycle. If the loading on the bus is light, this effectively keeps the data on the bus until the data bus is enabled to read the data, thus extending the data hold time for the previous write cycle. The effective hold time under these conditions will typically be >> 50 ns.

The data in Table 1 is preliminary and subject to revision.

Table 2. NEURON 3150 CHIP memory timing (worst-case @ 4.75V, 70°C).

Symbol	Parameter	Min	Max	Unit
t_{CYC}	Memory cycle time[1]	200	3200	ns
PW_{EH}	Pulse width ~E High	$t_{CYC/2}$ - 5	$t_{CYC/2}$ + 5	ns
PW_{EL}	Pulse width ~E low	$t_{CYC/2}$ - 5	$t_{CYC/2}$ + 5	ns
t_{AD}	Delay, ~E High to address valid	-	34	ns
t_{AH}	Address hold time	5	-	ns
t_{RD}	Delay, ~E high to R/~W valid (read cycle)	-	23	ns
t_{RH}	R/~W hold time (read cycle)	5	-	ns
t_{DSR}	Read data setup time	75	-	ns
t_{DZR}	Delay data bus high-Z to R/~W high	5	-	ns
t_{DHR}	Data hold time (read cycle)	0	-	ns
t_{WR}	Delay, ~E high to R/~W valid (write cycle)	-	23	ns
t_{WDD}	Delay, R/~W low to NEURON CHIP data drivers ON	10	-	ns
t_{DDW}	Delay, ~E low to data valid	-	64	ns
t_{WH}	R/-W hold time (write cycle)[2]	5	-	ns

Notes:

1. t_{cyc} = 2 x 1/f, where 'f' is the input clock frequency at CLK1. Valid values of 'f' are 10, 5, 2.5, 1.25, and .625 MHz.
2. If a write cycle is followed by a read cycle, the data bus goes to the high-impedance state at the beginning of the read cycle. If the loading on the bus is light, this effectively keeps the data on the bus until the data bus is enabled to read the data, thus extending the data hold time for the previous write cycle. The effective hold time under these conditions will typically be >> 50 ns.

The data in Table 2 is preliminary and subject to revision.

Memory Design Examples

Three example external memory configurations are detailed in the following sections.

Example 1 represents a minimum configuration using 32K bytes of external EPROM memory. This design can support a wide range of custom nodes which require less than 2K bytes of on-chip RAM for system and application data. The NEURON 3150 CHIP uses 16K bytes of the external EPROM memory to contain the NEURON CHIP firmware. The remaining 16K bytes of external EPROM space is available for application code and constants.

Example 2 shows a design that adds a 32K x 8 SRAM to the design shown in example 1. For nodes that may require more application and system data space than the 2K bytes on the 3150 chip, this design provides additional 32K bytes of RAM externally.

Example 3 replaces the 32K x 8 EPROM and the 32K x 8 SRAM with a single 32K x 8 NVRAM. This NVRAM provides the non-volatility needed by the system firmware and application code, as well as real-time re-writeability of any external locations used by variable application and system data. It also allows the developer to use the ability of the LONBUILDER Developer's Workbench to load application code *in situ* over the network.

These designs are shown only as examples. Many other configurations are also possible.

Example 1 - External Memory Interface with 32K x 8 EPROM

A memory design supporting a single-chip 32K x 8 EPROM device is shown in figure 4. This design uses a direct connection to the data bus with no external decoding logic. Up to 16K bytes of the EPROM are available for user application code and constants with this configuration.

Based on the timing information described earlier, an EPROM device with a 70 ns address access time is required for 10 MHz operation and a ± 10% power supply. A device with a 90 ns address access time is required for a ±5% power supply. At 5 MHz, a 250 ns access time is sufficient.

Suitable EPROM and one-time programmable (OTP) devices are listed at the end of this document. To reduce node cost for large-volume production, masked ROM devices could be substituted for the EPROM.

The data files needed to program the EPROM are created by the LONBUILDER Developer's Workbench in either Motorola S-record format or Intel Hex formats by exporting the application image.

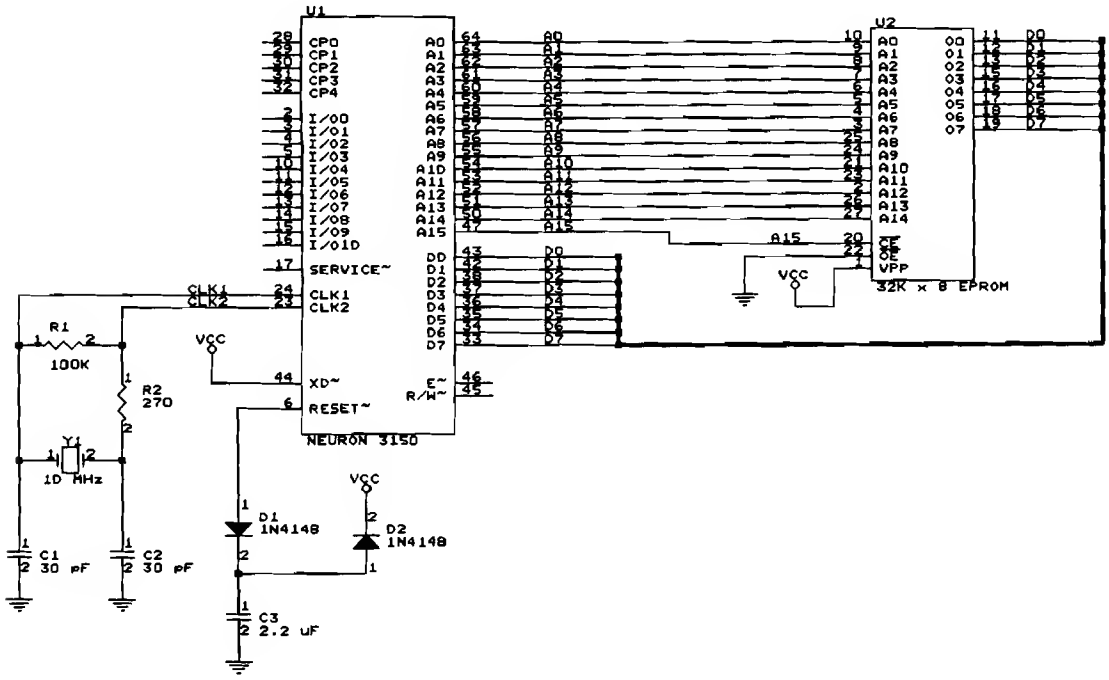

Figure 4. NEURON 3150 CHIP external memory interface with 32K byte EPROM.

Example 2 - External Memory Interface with 32K x 8 EPROM and 32K x 8 RAM

Applications requiring more than 2K bytes of RAM for system and application data space will require an external RAM device. Figure 5 shows an example design that adds a 32K x 8 static RAM chip to the previous design. With this design, the firmware, user application code, and user constants are stored in the EPROM. System and applications data are stored in the external RAM, in addition to using the 2K bytes on-chip RAM.

The NEURON 3150 CHIP reserves the upper 6K bytes of address space (E800H-FFFFH) for internal memory and I/O registers. When the NEURON 3150 CHIP reads from this address range, the external data bus is driven with the internally read data. If an external memory device is selected for this address range, there will be bus contention between the NEURON 3150 CHIP and the external device. To prevent this occurrance, gate U6A de-selects the external RAM for all addresses above E000H. The external RAM memory is therefore mapped to the address range 8000H-DFFFH, and the upper 8K bytes of the external RAM are unused. (This is 2K more than the 6K of contention area, but it greatly simplifies the control logic.)

Timing analysis for this design must include both read and write operations of the static RAM memory. The timing of the EPROM/ROM memory interface is identical to that described for example 1.

Reliable support of an external RAM is complicated by the fact that there is a gate between the ~E output of the NEURON 3150 CHIP and the ~WE input to the RAM. The minimum guaranteed address hold time from the NEURON 3150 CHIP is 5 ns, relative to ~E rising. The 74AS32 gate shown in the schematic in figure 5 has a maximum delay of 5.8 ns at minimum voltage and a 50 pF load. Further, delay characteristic curves for advanced Schottky devices show that AS drivers speed up approximately 20% at loads of 25 pF or less. (See figure 23 on page 4-21 of the 1986 Texas Instruments' *ALS/AS Logic Data Book*, or equivalent.) The load imposed by the RAM is 6 pF. Adding trace capacitance, the load driven by the output of the 74AS32 gate is less than 15 pF. In these conditions, the 74AS32 gate would exhibit a maximum delay of 4.6 ns.

To determine the speed requirement of the RAM, we must subtract the delay imposed by U4A, U5A, and U6A from available memory access 'window'. The longest delay of 13 ns occurs through the path encompassing U5A (8.5 ns) and U6A (4.5 ns). In a ±10% power supply system, the read access window becomes $t_{ACC} = t_{CYC} - t_{DSR} - t_{AD} - 13 = 200 - 83 - 38 - 13 = 66$ ns. A 55 ns RAM is the nearest industry-standard access speed meeting this timing requirement. In a ±5% power supply environment, the window is 91-13 = 78 ns. Thus a 70 ns RAM is sufficient. Running the NEURON 3150 CHIP at 5 MHz decreases the access time requirement for the RAM to 262 ns.

Suitable static RAM devices are listed at the end of this bulletin.

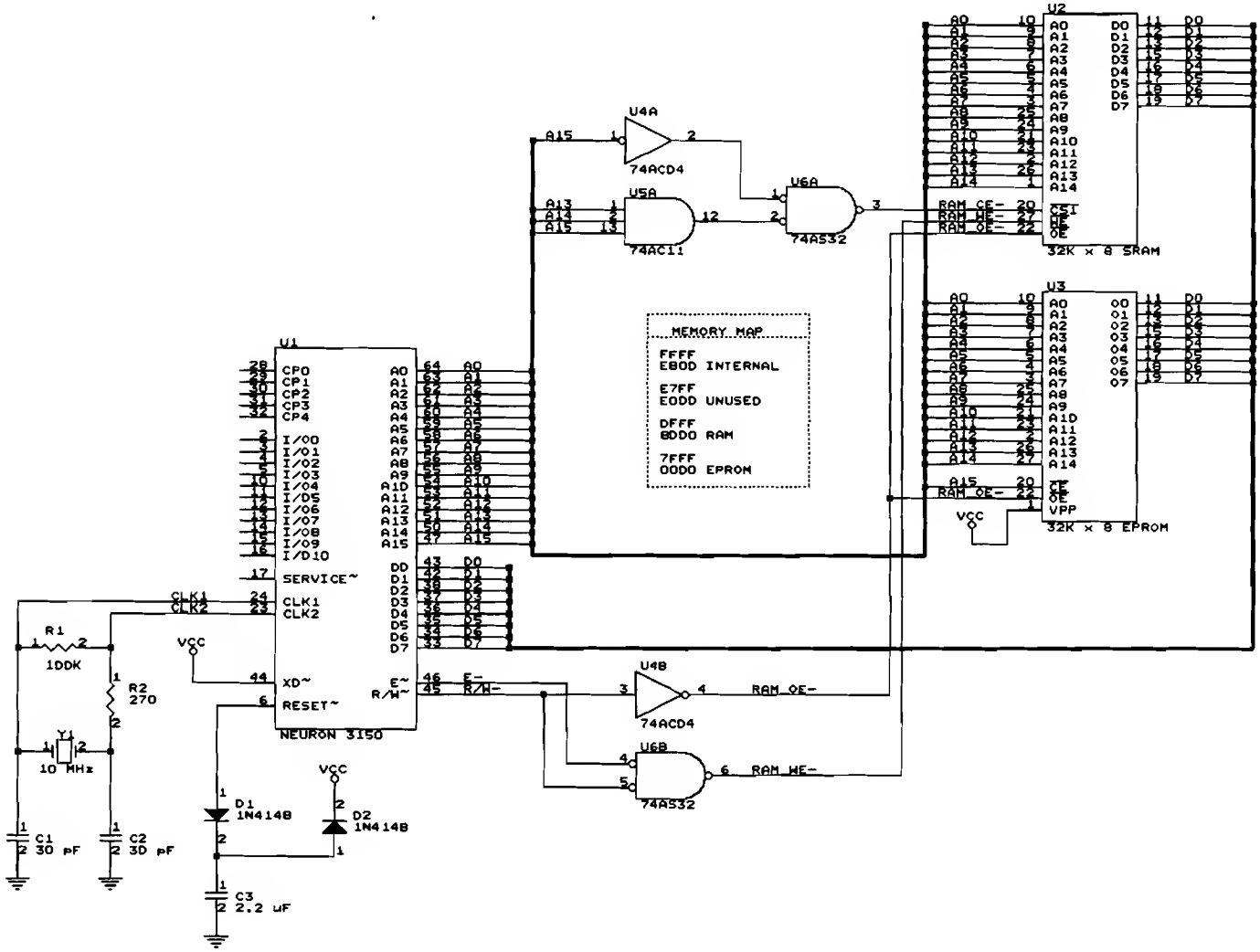

Figure 5. NEURON 3150 CHIP external memory interface with 32K byte EPROM and 32K byte RAM.

Example 3 - External Memory Interface with 32K x 8 Non-Volatile RAM

This example uses a single 32K x 8 non-volatile RAM (NVRAM) memory. Practical use of this circuit requires a PROM programmer which supports programming of the NVRAM devices to load the NEURON CHIP firmware. The remaining 16K bytes can be mapped as either RAM or off-chip EEPROM with a 0 write time. The calculation for the memory access time requirement is the same as that described in the previous example.

This design provides flexibility for prototype development of more complex applications. As mentioned on page 1, application program and data are written in non-volatile memory. The network download capability of the LONBUILDER system allows faster application code development as well as in-circuit modification with NVRAM. (EEPROMs cannot be written in-circuit due to their 20 ms write cycle time; EPROMs have to be taken out of the socket and re-programmed in a PROM programmer each time their contents have to be modified.) The schematic for this circuit is shown in figure 7. A design using external non-volatile memory must address the special requirements described in this section.

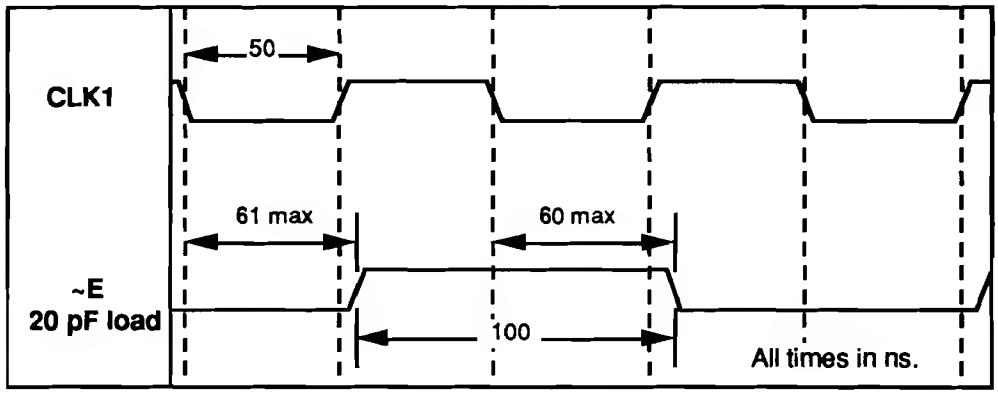

Figure 6. CLK1 and ~E timing relationships. The numbers shown (in ns) apply to CLK1 = 10MHz.

Reliable use of the NVRAM is more complicated than standard SRAM. This is due to the more stringent address hold time requirement of 5-20ns (depending on the vendor) for NVRAMs, compared to 0 for SRAMs. To compensate for this, two address latches, U1 and U2, are added to hold the address to the NVRAM stable well beyond the rising edge of RAM_WE-. The gating signal for the latches is the input clock to the NEURON CHIP (CLK1). For this reason, the clock circuit in this design uses a clock oscillator rather than a crystal or ceramic resonator. Figure 6 shows the relationship between CLK1 and ~E. The address latch is strobed twice for each memory cycle. However, as seen in figure 3, the address is stable both times. The addition of the address latches allows the propagation delay spec of the RAM_WE- gate. Thus, an 'AC32 gate can be used in place of an 'AS32 device.

When using a non-volatile memory, the system designer must protect against unwanted writes during critical transitions of the system's operation. During a software reset or a power cycle, the state of signal ~E is initially undefined, and can cause a spurious write to external memory by shortening the write enable signal while the address is changing. Failure to protect against such writes will corrupt an application program loaded in this memory. This is not a concern in the design shown in example 2 because the application program was not stored in RAM.

This design uses a 20V8 PAL device (U5) to provide combinatorial and registered logic to protect the non-volatile memory from spurious writes during unexpected power-down conditions, hardware reset, and software reset.

Execution of a software RESET instruction causes a write to address FFB4H, which is the mapped location of the NEURON 3150 CHIP's internal reset control register. Together, U3, U6, and U5 detect this event and preempt the NEURON 3150 CHIP by pulling the external ~RESET pin low. Just before U5 issues the external RESET, it disables all writes to the NVRAM, protecting it from corruption during the reset process. The PAL program for U5 is shown in table 3.

To protect the NVRAM during power-down cycles, this design incorporates two power monitoring devices. The first device (U7, Motorola MC34064) pulls its output low when the power supply voltage drops below 4.75 VDC. This signal is input to the PAL device, which waits for any current writes to complete before issuing a hardware reset to the NEURON 3150 CHIP.

Important Note: The voltage trip level of the MC34064 must be higher than that of the NVRAM's internal protection circuit. Otherwise, the NVRAM's internal protection could disable writes in the middle of a write cycle, which can result in a shortened write pulse to the NVRAM while the address is changing. For this reason, the NVRAM is selected to have a trip point lower than 4.75 volts. The second power monitoring device, a Dallas Semiconductor DS1231 (U10), is necessary to hold the ~RESET line down while the PAL device signals become unpredictable during the power fall. U10 also guarantees a reliable reset operation in the event of a power brownout, i.e., power dropping below 4 V but not below 2 V.

To allow the NEURON 3150 CHIP to settle down during power-up or re-start from reset, the PAL device is programmed to provide a simple state machine which disables writes to the RAM until two transitions of the NEURON 3150 CHIP ~E signal are detected. This guarantees the NEURON 3150 CHIP has stabilized after a critical transition.

Two suitable NVRAM devices for this design are listed at the end of this bulletin.

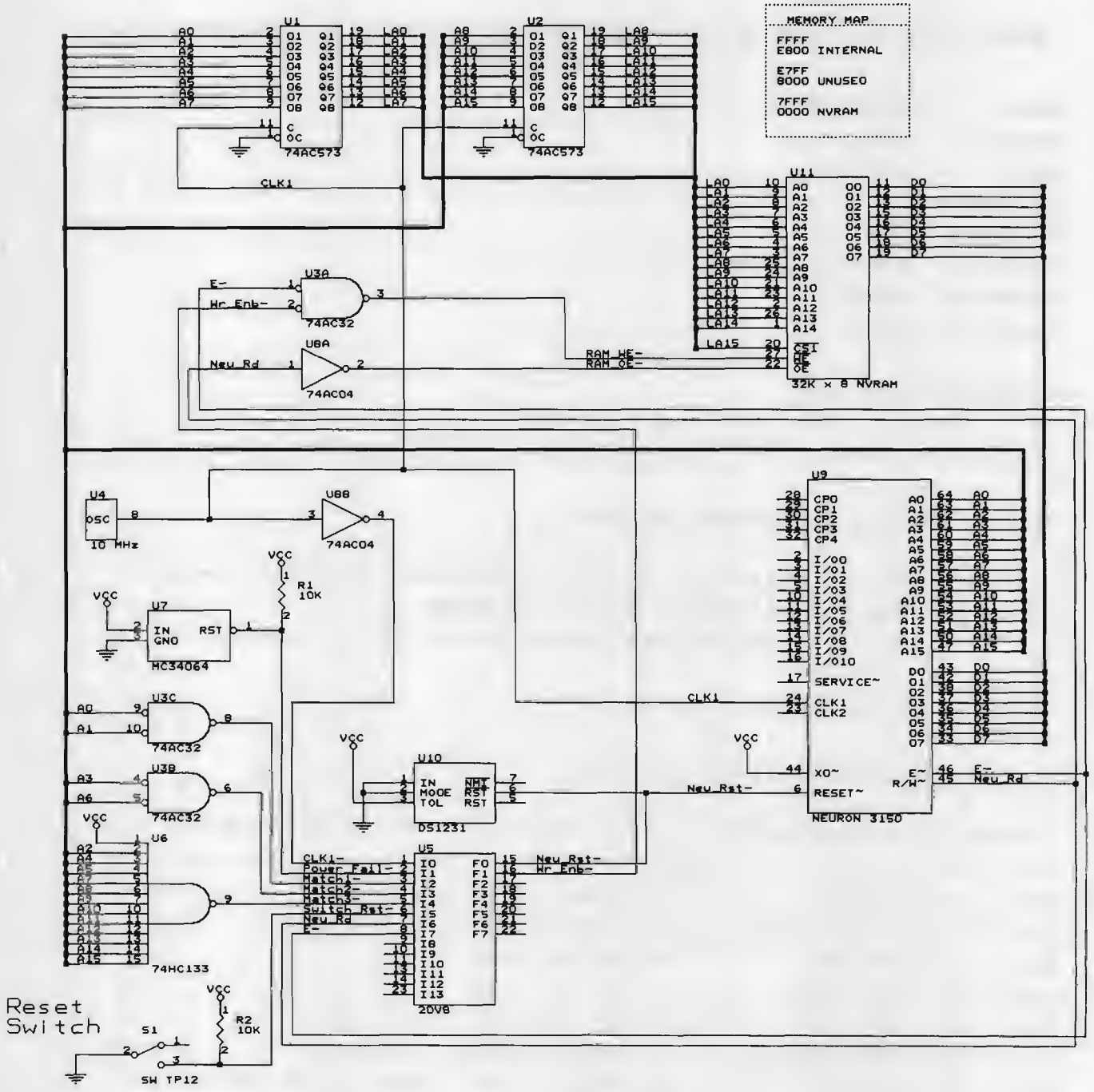

Figure 7. NEURON 3150 CHIP external memory interface with 32K byte NVRAM.

Table 3. PAL equations for the NVRAM reset and power-down protection circuits.

```
Name       NVRPROT;
PartNo     XXXX;
Date       8/8/91;
Revision   A;
Designer   KO;
Company    Echelon Corp.;
Assembly   XXXXX;
Location   XXXX;

$INCLUDE CTYPE.OPR

/*****************************************************************/
/*                                                               */
/*   Reset and Power-down Control                                */
/*                                                               */
/*****************************************************************/
/*  Allowable Target Device Type:  GAL20V8                       */
/*****************************************************************/
/*                                                               */
/* Revision History:                                             */
/*                                                               */
/*  A - Original Version  8/7/91                                 */
/*                                                               */
/*****************************************************************/
/*-----------------   Inputs  ---------------------------------*/
Pin    1 = !CLK1;           /* Clock input to Neuron            */
Pin    2 = !Power_Fail;     /* Power Fail from MC34064          */
Pin    3 = !Match1;         /* A0, A1 Low                       */
Pin    4 = !Match2;         /* A3, A6 Low                       */
Pin    5 = !Match3;         /* A2, A4, A5, A7-15 High           */
Pin    6 = !Switch_Rst;     /* Reset Switch Input               */
Pin    7 = Neu_Rd;          /* Read/Write- signal from Neuron   */
Pin    8 = !E_Clk;          /* Neuron E-Clk                     */
```

```
/*----------------------- Outputs ---------------------------*/

Pin   15 = !Neu_Rst;       /*  Open-drain reset line          */
Pin   16 = !Wr_Enb;        /*  NVRAM Write Enable             */
Pin   17 = Neu_Rst_Wrt;    /*  Intermediate term to reduce    */
                           /*  product terms in other pins    */
Pin   18 = Wr_Arm;         /*  Arming bit for enabling writes */
                           /*  to NVRAM                       */
Pin   20 = Rst_Restart1;   /*  Reset recovery wait register #1 */
Pin   21 = Rst_Restart2;   /*  Reset recovery wait register #2 */
Pin   22 = Rst_Flag;       /* Register that causes signal /Reset*/
                           /*  to be asserted                 */


/*----------- Definitions:  Intermediate Variables ----------*/

   /* External Reset is the OR of the reset switch and the    */
   /* Power-fail detector, each qualified with E_Clk.         */

Ext_Reset = Switch_Rst & E_Clk | Power_Fail & E_Clk;


   /*  Neuron software reset is detected by all three inputs  */
   /*  from the external address compare gates (Match1,2,3)   */
   /*  being true (low), Neu_Rd indicating a Neuron Write,    */
   /*  and E_Clk = true (low) to qualify the address.         */

Neu_SW_Rst = Neu_Rst_Wrt & E_Clk;

   /*  Neu_Rst is driven open-drain (equivalent) by tying its   */
   /*  input  true and modulating the three-state enable.       */

Neu_Rst.oe   = Rst_Flag;
Neu_Rst      = Rst_Flag;
Rst_Flag.D   = Neu_Rst_Wrt & E_Clk | Ext_Reset;
```

```
   /*  Neu_Rst_Wrt is not needed as a separate output except     */
   /*  to reduce the number of product terms down the line.      */
   /*  If a 22V10 part were being used, this pin could be        */
   /*  replaced by a simple intermediate declaration.            */

Neu_Rst_Wrt = Match1 & Match2 & Match3 & !Neu_Rd;

   /*  The Rst_Restart1,2 flags are used to hold off Write       */
   /*  Arm (Wr_Arm) until the Neuron has had a chance to         */
   /*  come up from reset and re-start E_Clk.  Since E_Clk is    */
   /*  high during reset, Rst_Restart1 looks for E_Clk to be     */
   /*  sampled low.  If E_Clk is sampled low three times, the    */
   /*  three signals Rst_Restart1, Rst_Restart2, and Wr_Arm      */
   /*  will come true one at a time, so Wr_Arm will go true      */
   /*  after the third sample of E_Clk low.  This is ample to    */
   /*  ensure that the Neuron has stabilized after restart.      */
   /*  Wr_Arm is then used to enable the Neuron Read/Write line  */
   /*  (Neu_Rd) out to the rest of the logic as Wr_Enb.          */

Rst_Restart1.D = E_Clk & !Neu_SW_Rst & !Switch_Rst & !Power_Fail
        | Rst_Restart1 & !Neu_SW_Rst & !Switch_Rst
        & !Power_Fail;

Rst_Restart2.D = E_Clk & Rst_Restart1 & !Neu_SW_Rst & !Switch_Rst
        & !Power_Fail | Rst_Restart2 & !Neu_SW_Rst  & !Switch_Rst
        & !Power_Fail;

Wr_Arm.D        = E_Clk & Rst_Restart2 & !Neu_SW_Rst & !Switch_Rst
        & !Power_Fail | Wr_Enb & !Neu_SW_Rst & !Ext_Reset;

Wr_Enb          = !Neu_rd & Wr_Arm;
```

NEURON 3150 CHIP Input Loading and Output Drive

The input characteristics of the NEURON 3150 CHIP for the memory interface pins are as follows:

Voltage levels = TTL

Input current = ± 10 μA with $V_{SS} < V_{IN} < V_{DD}$

All of the NEURON 3150 CHIP outputs used for memory interfacing have standard current drive capability, as follows:

V_{OL} = 0.4 V max at I_{OL} = 1.4 mA

V_{OH} = 2.4 V min at I_{OH} = -1.4 mA

Suitable Memory Devices

The following tables lists vendors whose product lines include parts meeting the performance demands of the NEURON 3150 CHIP operating at 10 MHz. The list does not cover all possible semiconductor manufacturers. Contact the individual manufacturers or their representatives for price and availability.

EPROM (32K X 8), 70 ns Access Time (10 MHz ± 10% Power Supply)

Microchip	27HC256-70
Catalyst	CAT27HC256L-70
Wafer Scale Integration	57C256F-70

EPROM (32K X 8), 90 ns Access Time (10 MHz ± 5% Power Supply)

Toshiba	TC57H256D-90
AMD	AM27C256-90
Amtel	AT27HC256-90

Static RAMs (32K X 8), 55 ns Access Time (10 MHz ± 10% Power Supply)

Motorola	MCM6206C-55
Texas Instruments	SM68CE256-55
IDT	IDT71256-55
Cypress Semiconductor	CY7C199-55

Non-Volatile RAM (10 MHz ± 10% Power Supply)

BENCHMARQ	bq4011HYMA-45

Non-Volatile RAM (10 MHz ± 5% Power Supply)

Dallas Semiconductor	DS1230Y-70

Part Number 005-0013-01

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